REMARKS/ARGUMENTS

1. Rejection of claims 1-5 under 35 U.S.C. 103(a):

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) further in view of Von Kaenel (US 2003/0067335).

Response:

The applicant would like to point out the patentable features of claim 1 below. Claim 1 recites the limitation of "a counter connected to the phase-frequency detector and the counter for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and generating a second counting value by counting the number of cycles of the reference clock during the duration of the second control signal". The decision logic circuit then generates a third counting value based on the first counting value and the second counting value which is later used for outputting the phase adjusting value.

On the other hand, none of the cited prior art references teach a counter for "generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and generating a second counting value by counting the number of cycles of the reference clock during the duration of the second control signal".

As noted by the Examiner, Hsu does not teach a counter as claimed.

Takumai teaches in paragraph [0075] that "The internal counter 271 performs a counting operation in a time period, during which one of the first phase difference detection signal and second phase difference detection signal maintains a high level".

Thus, Takumai teaches that the counter only generates one counting value, and does not teach generating both a first counting value and a second counting value, as is claimed.

Von Kaenel also teaches that the counter 14 shown in Figure 1 generates only a single counting value.

Therefore, none of the cited prior art references teach the claimed counter "for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and generating a second counting value by counting the number of cycles of the reference clock during the duration of the second control signal". As a result, the applicant submits that claim 1 is patentable over the combination of Hsu, Takumai, and Von Kaenel. Claims 2-5 are dependent on claim 1, and should be allowed if claim 1 is allowed. Reconsideration of claims 1-5 is therefore respectfully requested.

2. Rejection of claim 6 under 35 U.S.C. 103(a):

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) further in view of Von Kaenel (US 2003/0067335), and further in view of Fukuhara (2002/0027966).

Response:

Claim 6 is dependent on claim 1, and should be allowed if claim 1 is allowed. Reconsideration of claim 6 is therefore respectfully requested.

3. Rejection of claims 7, 13, 14, and 20 under 35 U.S.C. 103(a):

Claims 7, 13, 14, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US

2003/0081516).

Response:

Claims 7 and 14 have been amended to overcome these rejections. Claim 7 now contains the limitations previously found in claim 8, and claim 14 now contains the limitations previously found in claim 15. No new matter has been added through the claim amendments.

Like claim 1, claim 7 now recites "a counter connected to the phase-frequency detector and the clock generator for generating a first counting value by counting the number of cycles of the second reference clock during the duration of the first control signal, and generating a second counting value by counting the number of cycles of the second reference clock during the duration of the second control signal".

Similarly, claim 14 states the steps of "generating a first counting value by counting the number of cycles of a second reference clock during the duration of the first control signal" and "generating a second counting value by counting the number of cycles of the second reference clock during the duration of the second control signal".

As none of the cited prior art references teach generating the first counting value and the second counting value as claimed, the applicant respectfully submits that each of the currently amended claims 7 and 14 are patentable over the cited prior art.

Furthermore, claims 13 and 20 are dependent on claims 7 and 14, and should be allowed if their respective base claims are allowed. Reconsideration of claims 7, 13,

14, and 20 is therefore respectfully requested.

4. Rejection of claims 8-11 and 15-18 under 35 U.S.C. 103(a):

Claims 8-11 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) further in view of Von Kaenel (US 2003/0067335), and further in view of Fukuhara (2002/0027966).

Response:

Claims 8 and 15 have been cancelled, and are no longer in need of consideration. Claims 9-11 and 16-18 are dependent on claims 7 and 14, and should be allowed if their respective base claims are allowed. Reconsideration of claims 9-11 and 16-18 is therefore respectfully requested.

5. Rejection of claims 12 and 19 under 35 U.S.C. 103(a):

Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) further in view of Nakao et al. (5,939,947).

Response:

The applicant would like to point out how claims 12 and 19 are patentable over the cited prior art. Claim 12 recites the limitations of "a comparator connected to the counter and the register for generating an enable signal when the cycle number of the first reference clock is equal to the phase adjusting value" and "a pulse generator connected to the comparator for generating an impulse when receiving the enable signal".

In a similar manner, claim 19 recites the steps of "generating an enable signal

when the cycle number of the first reference clock is equal to the phase adjusting value" and "generating an impulse when receiving the enable signal".

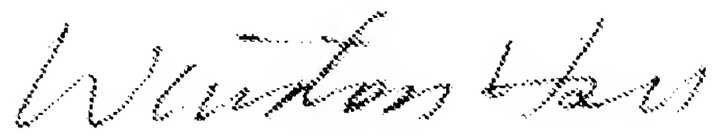
On the other hand, Nakao does not teach a comparator that generates an enable signal when the cycle number of the first reference clock is equal to the phase adjusting value. The Examiner has stated that element 3B in Figure 1 of Nakao is a comparator. However, element 3B is merely a delay element, as Nakao explains in column 4, lines 1-2. Another instance where the reference number "3B" is written in column 4, line 9 is actually a typographical error, and the "frequency comparing unit 3B" should actually read as "frequency comparing unit 38" instead.

Because Nakao does not teach a comparator that generates an enable signal when the cycle number of the first reference clock is equal to the phase adjusting value, Nakao also does not teach generating an impulse when receiving the enable signal. For these reasons, the applicant submits that both claims 12 and 19 are patentable over the cited prior art.

In addition, claims 12 and 19 are dependent on claims 7 and 14, and should be allowed if their respective base claims are allowed. Reconsideration of claims 12 and 19 is therefore respectfully requested.

In view of the claim amendments and the above arguments in favor of patentability, the applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,



Date: 10.12.2007

Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)